AMENDMENTS

In the Claims:

Please amend claim 20 as follows. Pursuant to the revised format for amendments, the status of each claim is set forth below.

1-8. (Cancelled)

9. (Previously Presented) A method of manufacturing a semiconductor device comprising at least first and second MOS transistors, said method comprising:

(a) providing a semiconductor substrate having at least first and second active regions of a first conductivity type and at least third and fourth active regions of a second conductivity type opposite to said first conductivity type;

(b) forming a gate oxide layer having a first thickness onto at least said first, second, third and fourth active regions;

(c) forming an electrode layer of non-doped polysilicon onto said gate oxide layer;

(d) patterning said electrode layer to form first, second, third and fourth gate electrodes onto said first, second, third and fourth active regions, respectively;

(e) doping said first active region and said first gate electrode with an impurity of said second conductivity type to form a first transistor driven at a first voltage level, said first gate electrode being doped at a first concentration;

(f) doping said second active region and said second gate electrode with an impurity of said second conductivity type to form a second transistor to be driven at a second voltage level lower than said first voltage level, said second gate electrode being doped at a second concentration higher than said first concentration;

(g) doping said third active region and said third gate electrode with an impurity of said first conductivity type to form a third transistor to be driven at said first voltage level, said third gate electrode being doped at a third concentration; and

(h) doping said fourth active region and said fourth gate electrode with an impurity of said first conductivity type to form a fourth transistor to be driven at said second voltage level, said fourth gate electrode being doped at a fourth concentration higher than said third concentration.

10. (Previously Presented) The method of claim 9, wherein said doping steps (e) to (h) comprise implanting ions of an impurity in said active regions and said gate electrodes.

11. (Previously Presented) The method of claim 9, wherein said lower concentration of impurities in said first and third gate electrodes causes the creation of a depletion layer in said first and third gate electrodes when a driving voltage is applied thereto.

12. (Previously Presented) The method of claim 9, wherein said first active region and said first gate electrode are doped simultaneously.

13. (Previously Presented) The method of claim 9, wherein said second active region and said second gate electrode are doped simultaneously.

14. (Previously Presented) The method of claim 9, further including the step of forming a gate oxide under each of said gate electrodes.

15. (Previously Presented) The method of claim 14, wherein all of said gate oxides are the same thickness.

16. (Previously Presented) The method of claim 15, wherein all of said gate oxides have a shape wherein they are thicker at side edges of said gate electrodes than at the center thereof.

17. (Previously Presented) The method of claim 16, further including oxidizing said side walls of said gate electrodes, said gate oxides under each of said gate electrodes being thickened at edge portions while said side walls are oxidized.

18. (Previously Presented) The method of Claim 9, said method further comprising:

oxidizing said first and second gate electrodes to form an oxide film under said gate electrodes, said oxide film being thicker at an edge portion than at a center portion of said gate electrodes.

19. (Previously Presented) The method of claim 11, wherein the depletion region in the gate electrode makes a dielectric breakdown voltage between the gate electrode and the active region higher.

20. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

(a) doping an active region and gate electrode of a high voltage CMOS circuit at a low impurity concentration; and

(b) doping an active region and gate electrode of a low voltage CMOS circuit at a high impurity concentration after said step (a),

to provide a high voltage CMOS circuit having enhanced gate oxide breakdown voltage due to a lightly doped gate electrode relative to the low voltage CMOS circuit.

21. (Previously Presented) The method of claim 21, further comprising:

(c) forming a sidewall spacer after said step (a) and before said step (b).

22. (Previously Presented) The method of claim 9, wherein said fourth active region and said fourth gate electrode are doped simultaneously.